From bottom to top: Exploiting hardware side channels in web browsers

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Secure Systems group

+ Secure Systems team: Daniel Gruss, Michael Schwarz, Peter Pessl

Introduction

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- information leaks because of the underlying hardware
- these vulnerabilities can also be exploited at a high level
- like a web browser
- because JavaScript is nothing more than code executing on your machine :)

Outline

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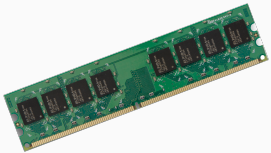
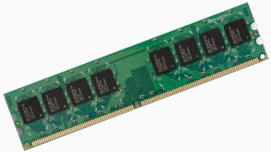
2. How can I use DRAM to create a covert channel?



Outline

1. What are micro-architectural side channels?
2. How can I use DRAM to create a covert channel?
3. How can I do that in JavaScript?!



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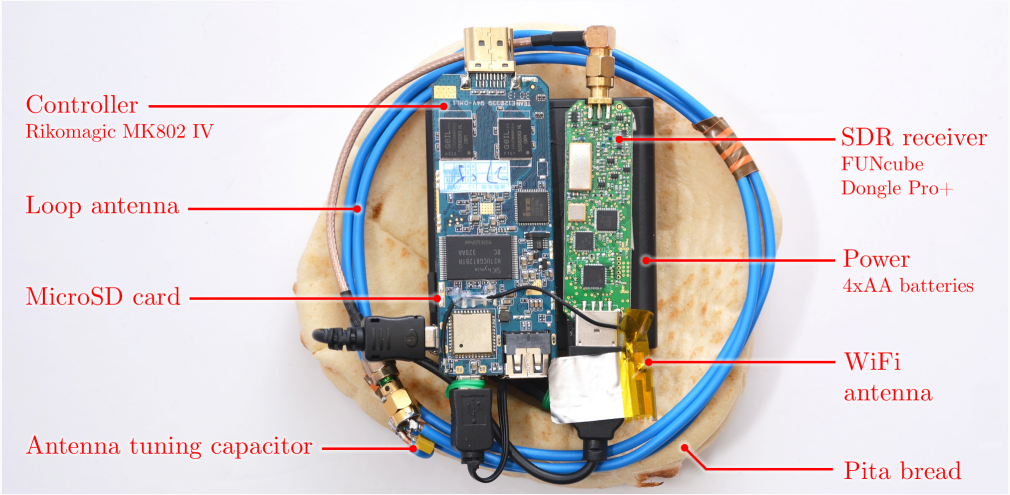

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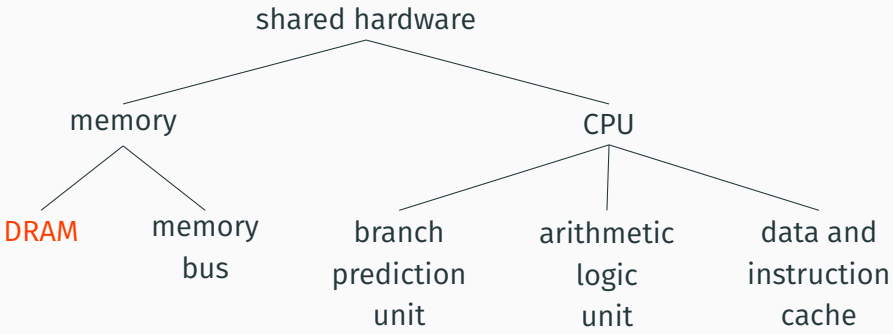
  → remote attacks

Shared hardware



DRAM and side channels

DRAM organization

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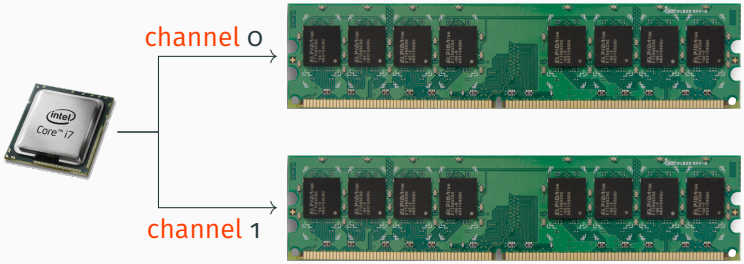

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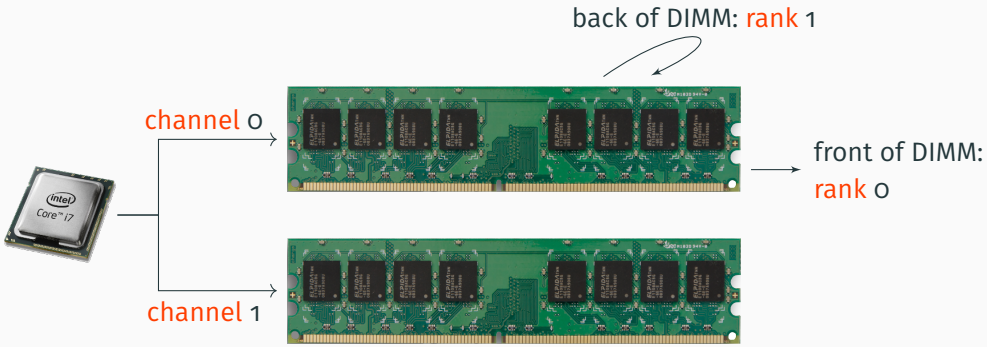

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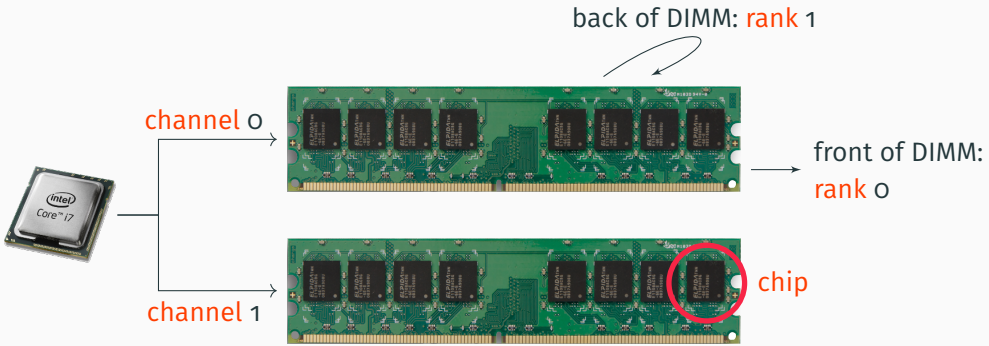
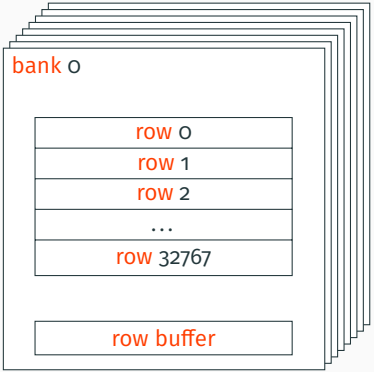


DRAM organization

chip



DRAM organization

chip

bank 0

row 0
row 1
row 2
…
row 32767

row buffer

64k cells
1 capacitor,
1 transitor each

DRAM row buffer

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- buffer the bits when reading them from the cells
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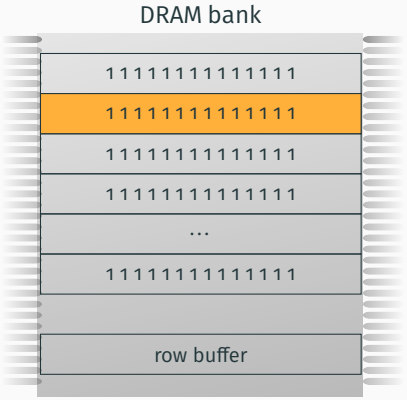
→ row buffer

How reading from DRAM works



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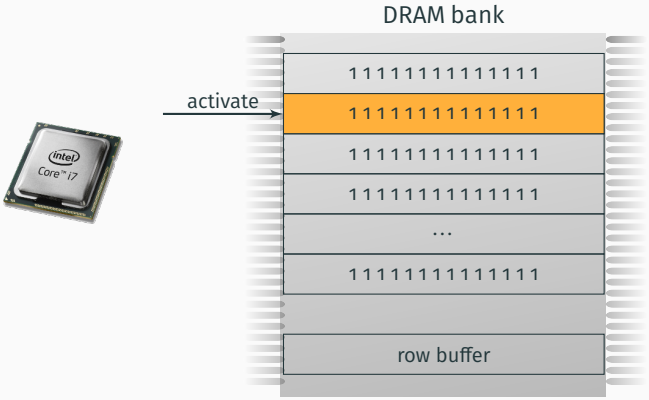

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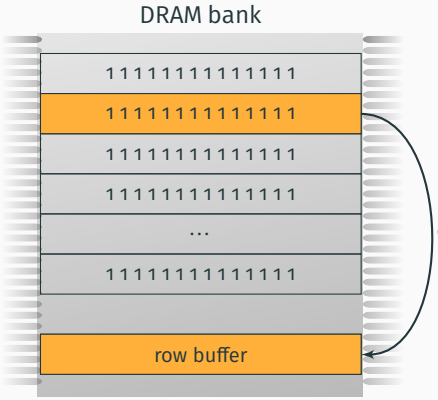

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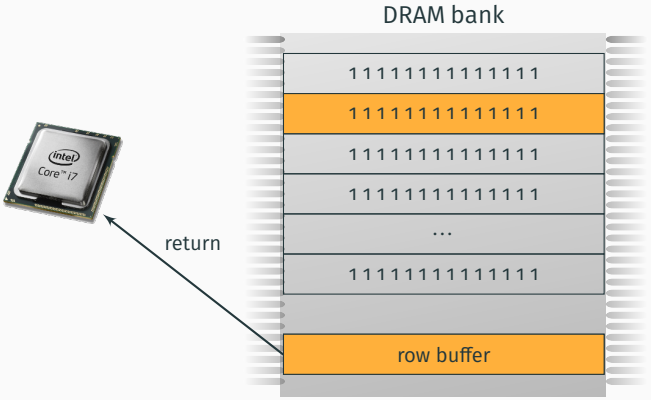

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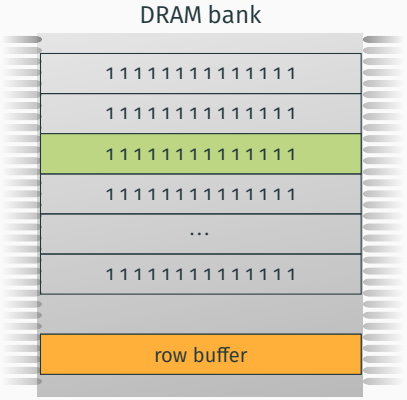

CPU wants to access row 2

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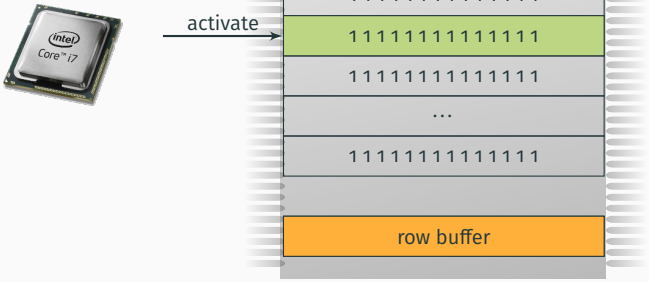

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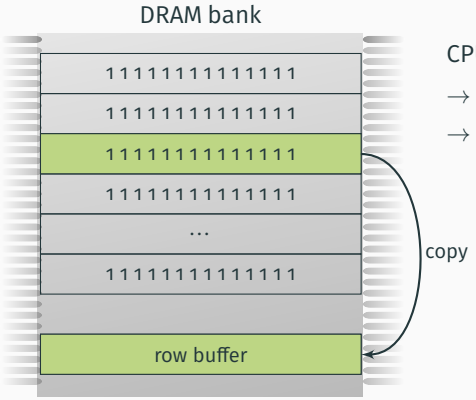

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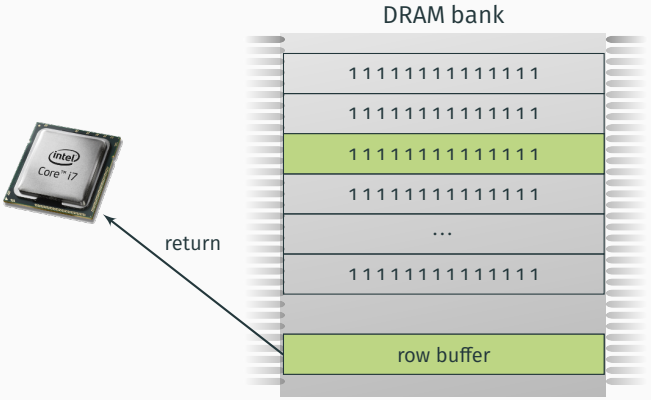

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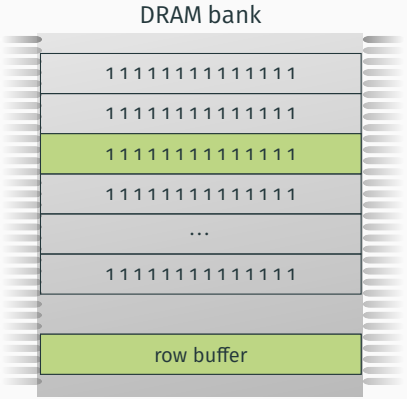

CPU wants to access row 2

→ row 2 activated

→ row 2 copied to row buffer

→ slow (row conflict)

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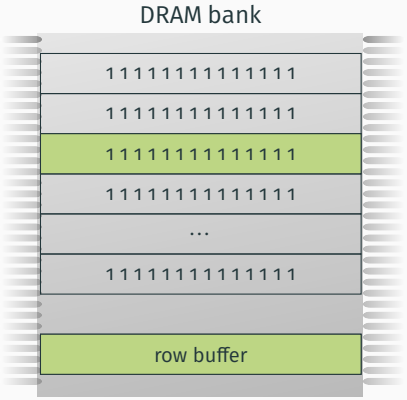

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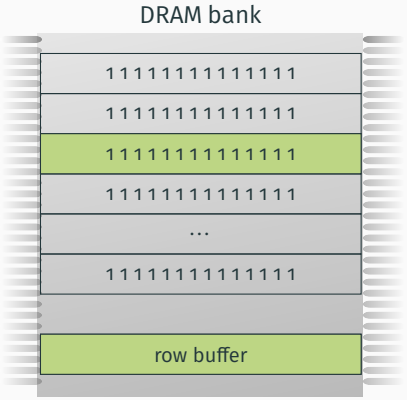

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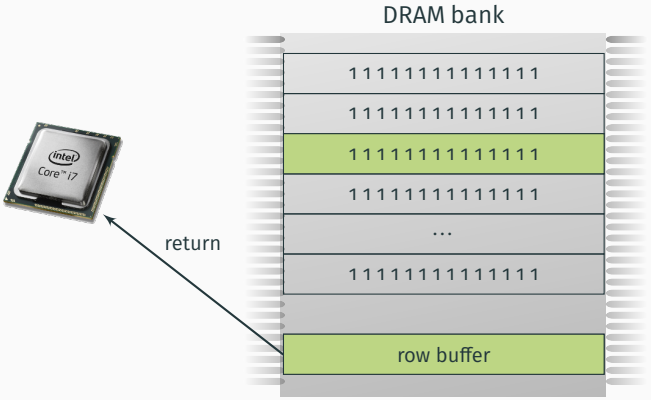

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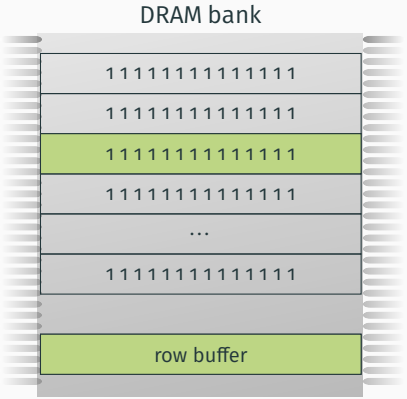

CPU wants to access row 2—again

→ row 2 already in row buffer

→ fast (row hit)

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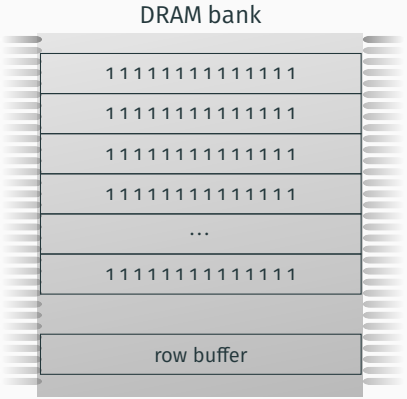
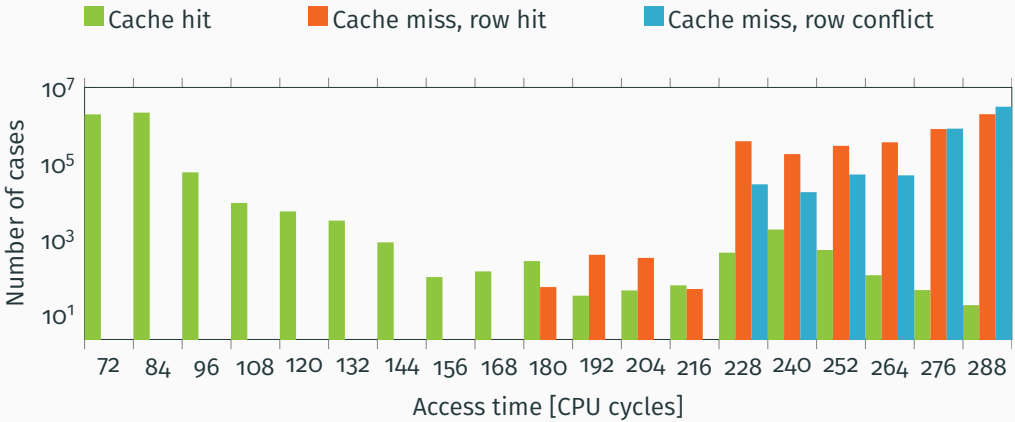


row buffer = cache

DRAM timing differences



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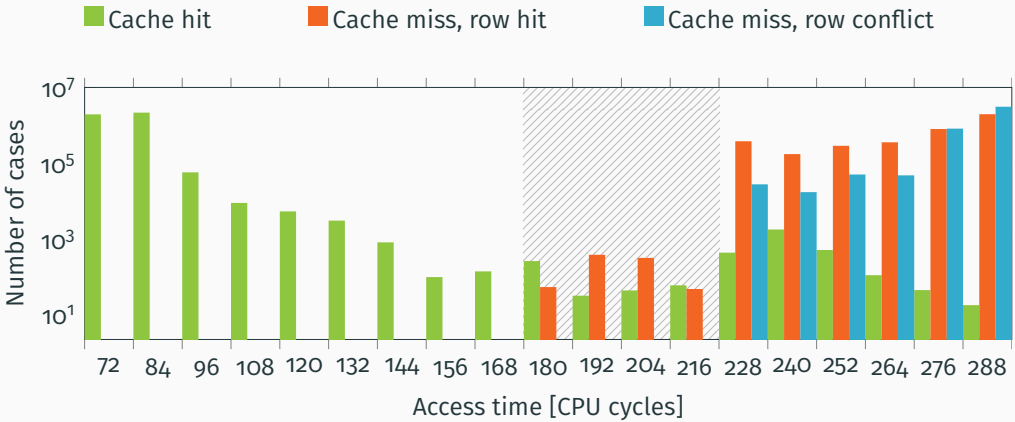

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→ we reverse-engineered them! `https://github.com/IAIK/drama`

P. Pessl et al. “DRAMA: Exploiting DRAM Addressing for Cross-CPU Attacks”. In: *USENIX Security Symposium*. 2016

DRAMA: DRAM Addressing attacks

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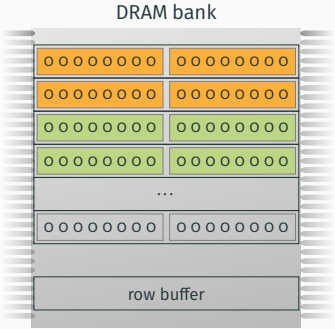
- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs
- side-channel attack: one malicious process spies on benign processes
  - e.g., spies on keystrokes

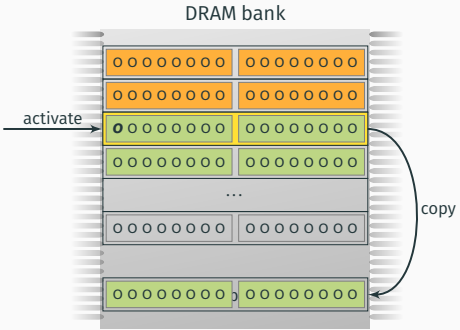
DRAMA covert channel



sender and receiver agree on one bank

receiver continuously accesses a row *i*

DRAMA covert channel



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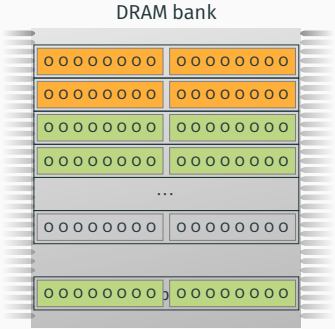

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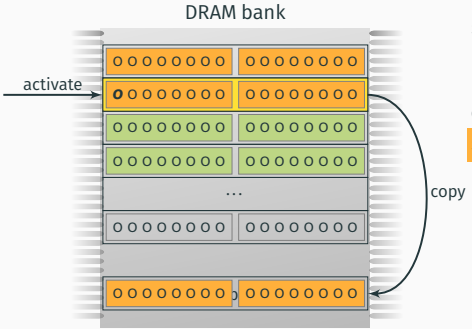

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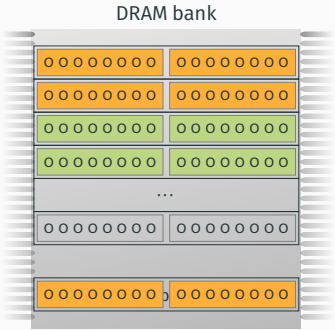

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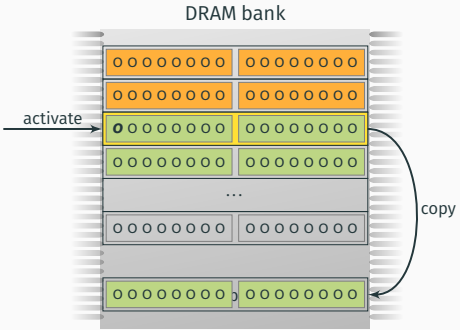

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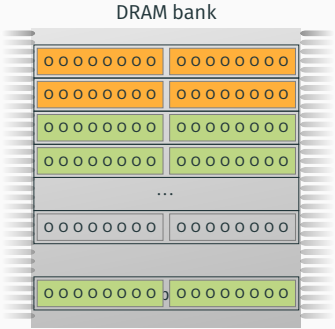

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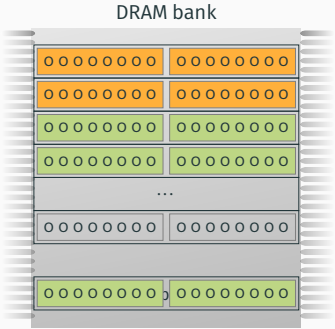
next receiver access $\rightarrow$ copy row buffer

$\rightarrow$ **slow**

DRAMA covert channel



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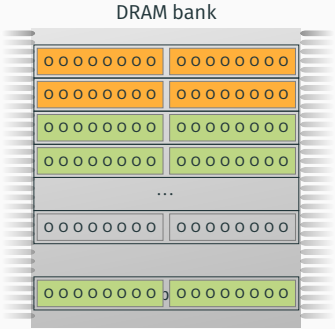
case #2: sender transmits o

DRAMA covert channel



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sender does nothing

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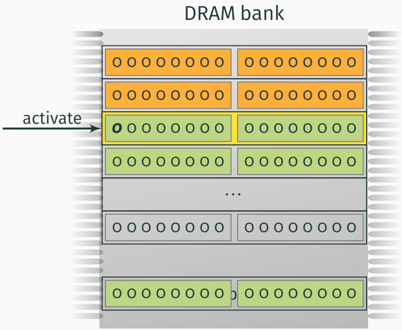

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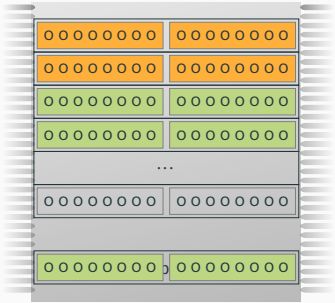
DRAMA covert channel

DRAM bank



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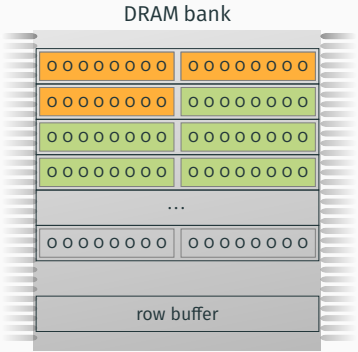
→ **fast**

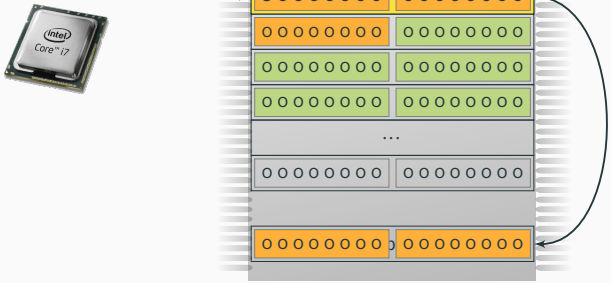
Two applications can covertly communicate with each other
But can we use that for spying?

DRAMA side-channel attacks



spy and victim share a row *i*

DRAMA side-channel attacks



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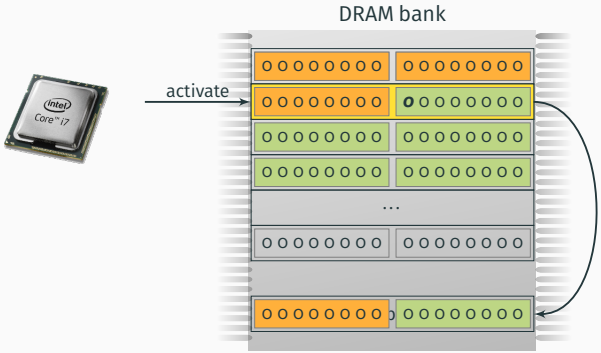

spy and victim share a row *i*

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victim accesses row *i*, copy to row buffer

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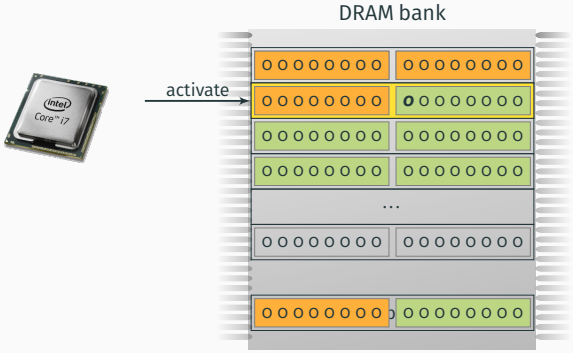

spy and victim share a row *i*

case #1

spy accesses row $j \neq i$, copy to row buffer
victim accesses row *i*, copy to row buffer
spy accesses row *i*, no copy

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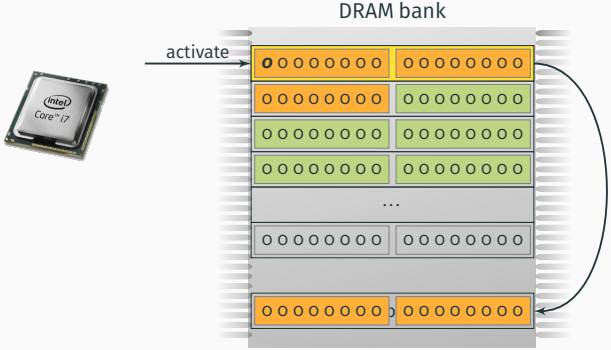

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case #2

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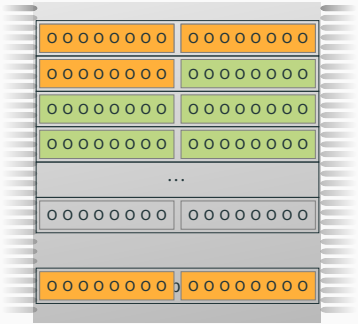
DRAMA side-channel attacks

DRAM bank



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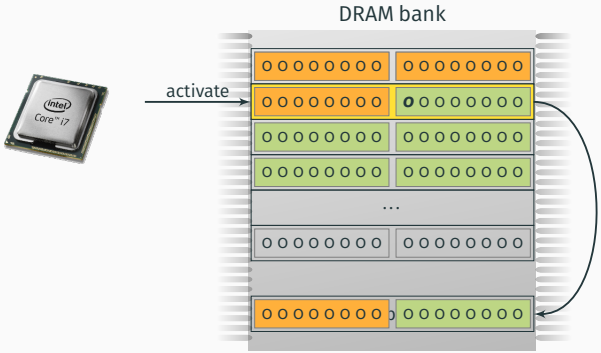

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case #2

spy accesses row $j \neq i$, copy to row buffer

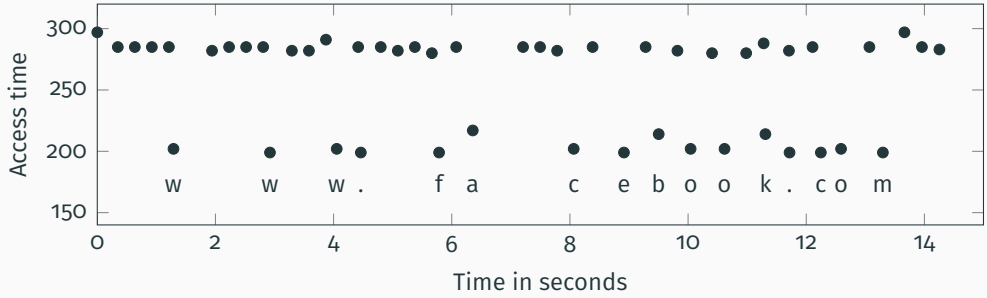
no victim access on row *i*

spy accesses row *i*, copy to row buffer

$\rightarrow$ **slow**

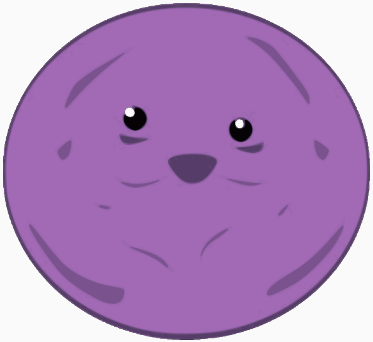
Spying on keystrokes on the Firefox URL bar

- side-channel: template attack
  - allocate a large fraction of memory to be in a row with the victim
  - profile memory and record row-hit ratio for each address



I’m sure we’ll need to write a lot of C code
At least we’re safe with JavaScript!

Member Rowhammer.js?



DRAM covert channels in JavaScript?

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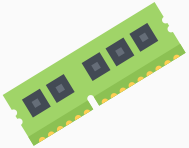
  1. accessing their own memory
  2. measuring time

Challenges with JavaScript



1. No knowledge about physical addresses

2. No instruction to flush the cache

3. No high-resolution timers

#1. No knowledge about physical addresses

- OS optimization: use Transparent Huge Pages (THP, 2MB pages)
- last 21 bits (2MB) of physical address
- = last 21 bits (2MB) of virtual address

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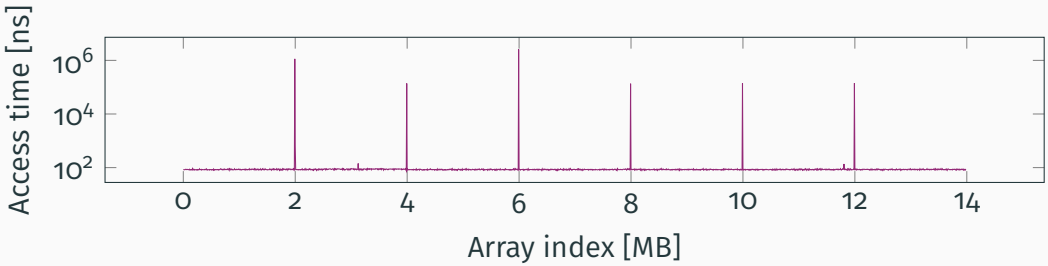
→ which JS array indices?

#1. Obtaining the beginning of a THP



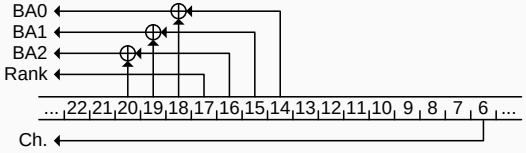
- physical pages for these THPs are mapped on-demand

→ page fault when an allocated THP is accessed for the first time

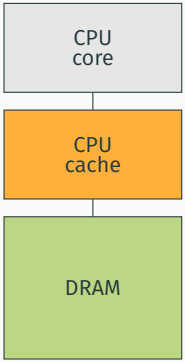
D. Gruss et al. “Practical Memory Deduplication Attacks in Sandboxed JavaScript”. In: *ESORICS’15*. 2015.

#1. Choosing physical addresses

- we now know the last 21 bits of physical addresses
- enough for most systems, e.g., Sandy Bridge with DDR3



#2. No instruction to flush the cache



- measure DRAM timing
- only non-cached accesses reach DRAM
- no `clflush` instruction

$\rightarrow$ evict data with other memory accesses

#2. Bypassing the CPU cache: Basic idea

- evicting cache line only using memory accesses

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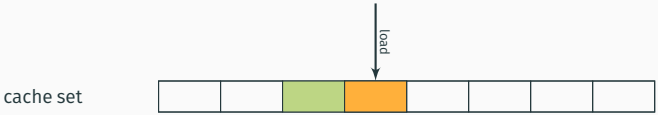

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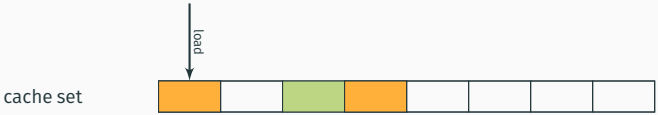

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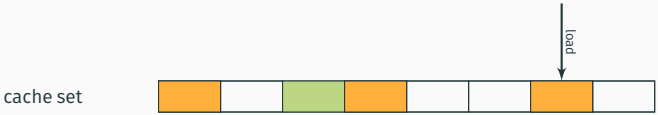

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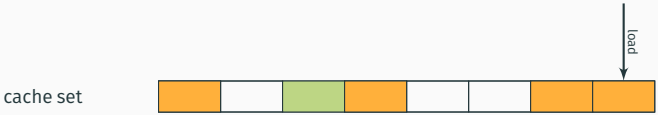

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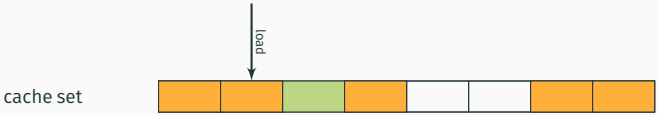

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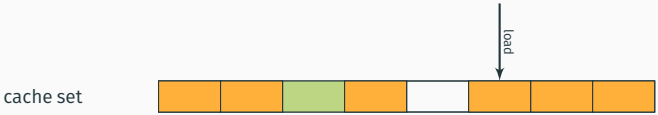

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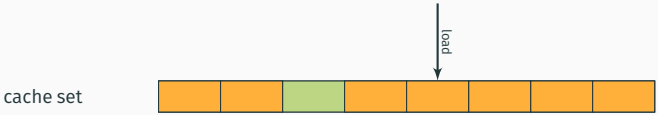

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- it's a bit more complicated than that: replacement policy is not LRU

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#2. Bypassing the CPU cache: Basic idea

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- it's a bit more complicated than that: replacement policy is not LRU
- but we already solved this problem before :)

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#3. High-resolution timers?

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`performance.now()`

[...] represent times as floating-point numbers with up to microsecond precision.

— Mozilla Developer Network

High-resolution timers in JavaScript

It was better before

- before September 2015: `performance.now()` had a nanosecond resolution

Y. Oren et al. “The Spy in the Sandbox: Practical Cache Attacks in JavaScript and their Implications”. In: *CCS’15*. 2015.

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- “fixed” in Firefox 41: rounding to 5 µs

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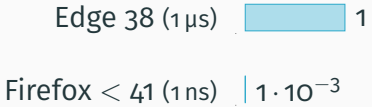
Microsecond precision?

Firefox < 41 (1 ns)	$1 \cdot 10^{-3}$

Microsecond precision?



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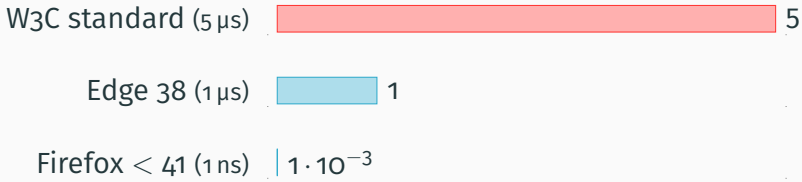

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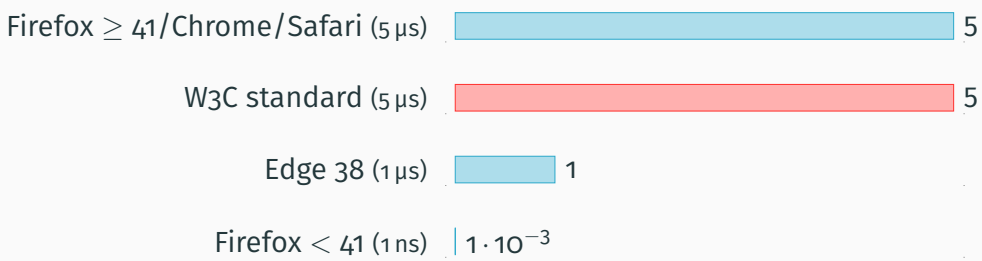

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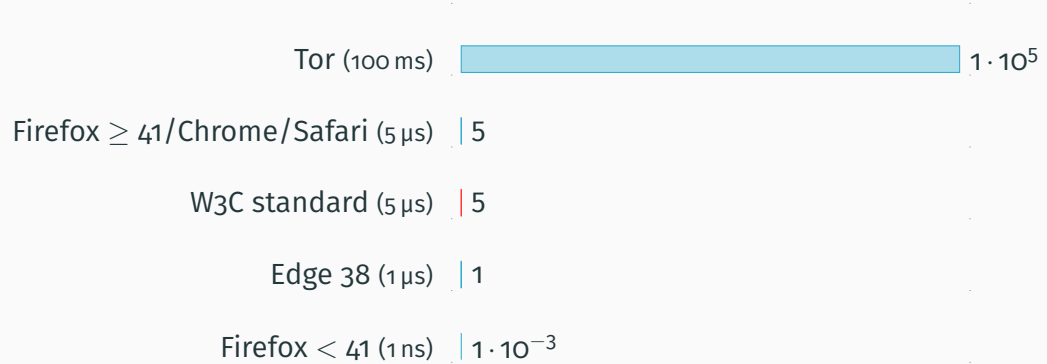

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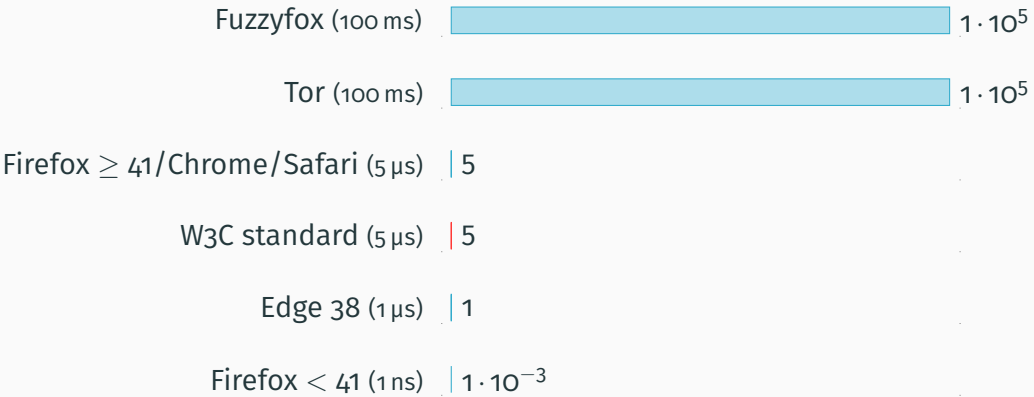

D. Kohlbrenner et al. “Trusted Browsers for Uncertain Times”. In: *USENIX Security Symposium*. 2016

We can do better!

- microsecond resolution is not enough

M. Schwarz et al. “Fantastic Timers and Where to Find Them: High-Resolution Microarchitectural Attacks in JavaScript”. In: *FC’17*. 2017.

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  2. build our own high-resolution timer

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Recovering resolution: Clock interpolation

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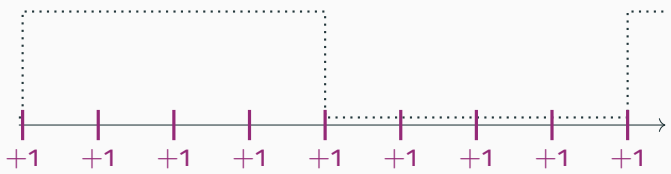

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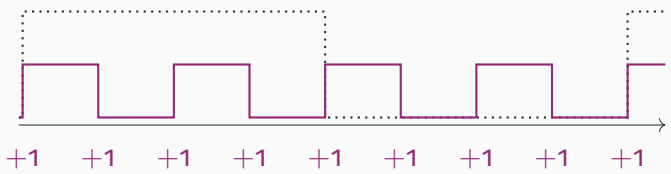

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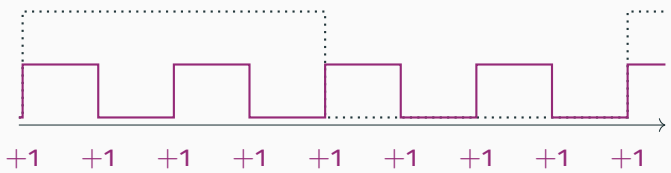

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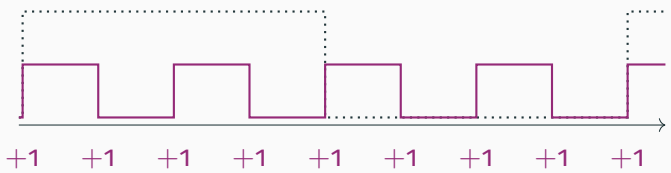

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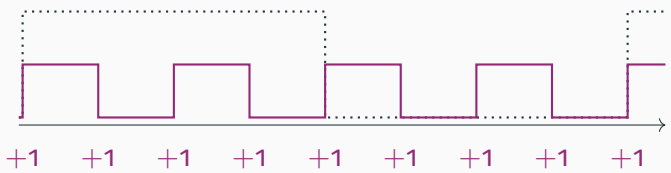

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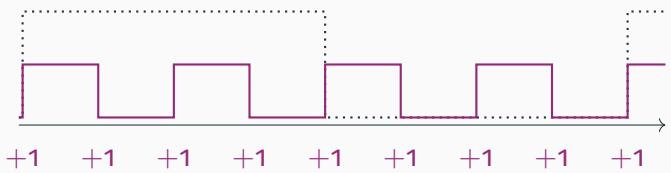

- to measure with high resolution
  - start measurement at clock edge
  - increment a variable until next clock edge
- Firefox/Chrome: 500 ns, Tor: 15 µs

Recovering resolution: Edge thresholding

- often sufficient to just see which of two functions takes longer

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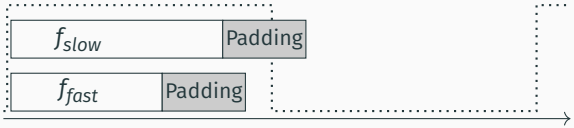
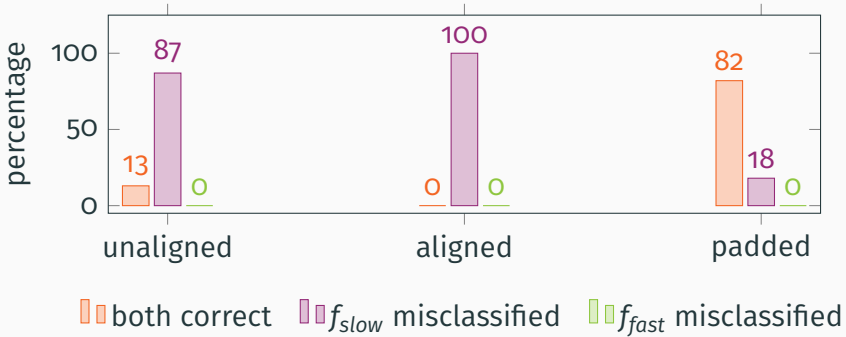


→ padding so the slow function crosses one more clock edge than the fast one

Recovering resolution: Edge thresholding



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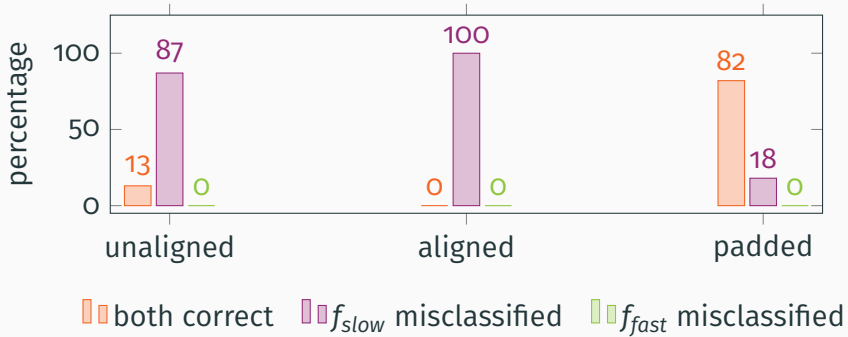

- nanosecond resolution

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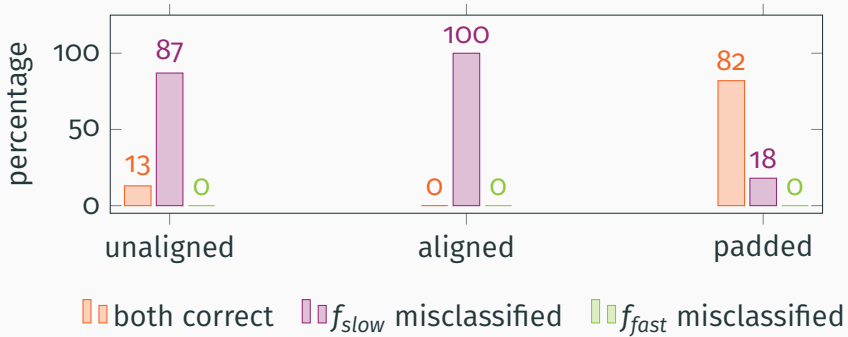

- nanosecond resolution
- Firefox/Tor: 2 ns, Edge: 10 ns, Chrome: 15 ns

Building a timer

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- CSS animation $\rightarrow$ increase width of element as fast as possible
- timestamp = width of element
- but animation limited to 60 fps $\rightarrow$ 16 ms resolution

Building a timer: Web worker

- JavaScript can spawn new threads called web worker

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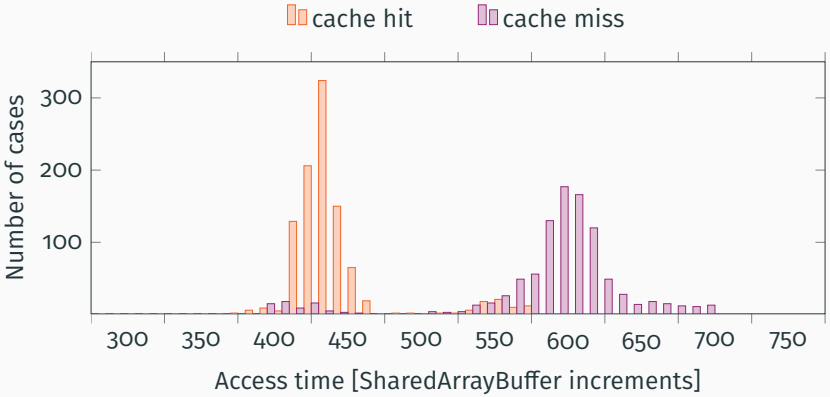
- Firefox/Fuzzyfox: 2 ns, Chrome: 15 ns

Building a timer: Is it good enough?



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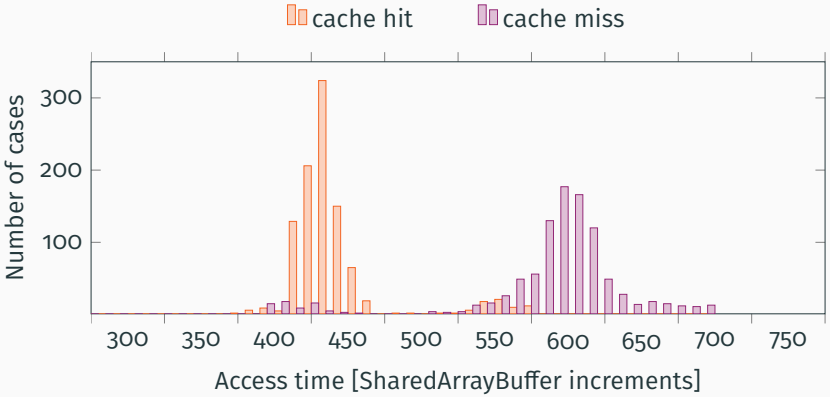

→ we can distinguish cache hits from cache misses (only ≈ 150 cycles difference)!

Take-away

Bonus: What else can we do with this?

- idea is not new: Wray (1992)
- we also exploited it in other contexts
  - on ARM
  - inside an SGX enclave

J. C. Wray. “An analysis of covert timing channels”. In: *Journal of Computer Security* 1.3-4 (1992), pp. 219–232.

M. Lipp et al. “ARMageddon: Cache Attacks on Mobile Devices”. In: *USENIX Security Symposium*. 2016.

M. Schwarz et al. “Malware Guard Extension: Using SGX to Conceal Cache Attacks”. In: *DIMVA’17*. 2017.

DRAM covert channels in JavaScript!

Setup

- sender: native application in a VM

Setup

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- receiver: JavaScript in a web page on the host

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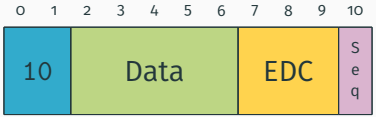
- sender and receiver select a different row inside this bank
- sender transmits 0 by doing nothing and 1 by causing row conflict
- receiver measures access time for its row: fast $\rightarrow$ 0, slow $\rightarrow$ 1

Sending packets



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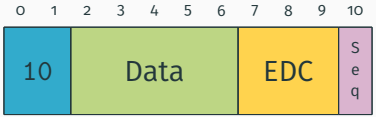
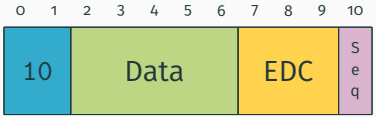
Sending packets



- communication based on 11-bit packets, with 5-bit of data
- packet starts with a 2-bit preamble

Sending packets



- communication based on 11-bit packets, with 5-bit of data
- packet starts with a 2-bit preamble
- data integrity checked by an error-detection code

Sending packets

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- packet starts with a 2-bit preamble
- data integrity checked by an error-detection code
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Evaluation

- transmission of approximately 11 bits/s

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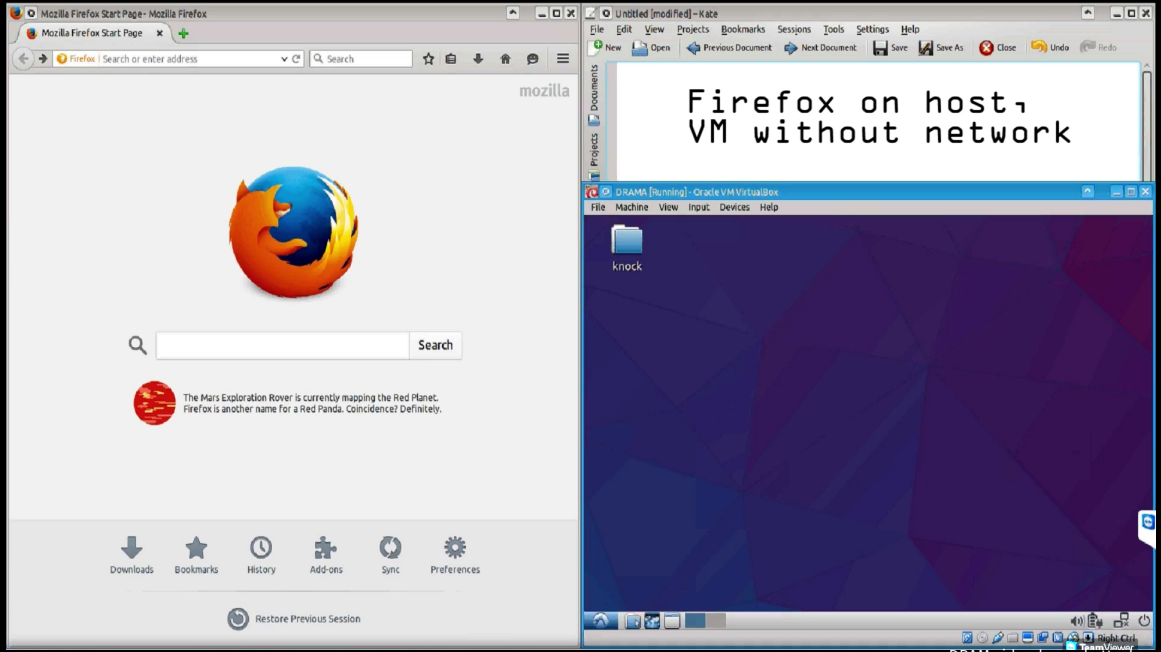
- native code: 596 kbit/s cross CPU and cross VM



DRAM side-channel attack

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- information leaks because of the underlying hardware
- vulnerabilities exploitable at the browser level
- running arbitrary JavaScript allows building high-resolution timers
- hard to mitigate without reducing functionality

Thank you!

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From bottom to top: Exploiting hardware side channels in web browsers

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